LISTING OF THE CLAIMS (not currently amended)

1. (Previously Presented) A memory cell formed of complementary NMOS and PMOS transistors, comprising:

a first inverter having a first output node, a first NMOS transistor and a first PMOS transistor, the first output node located between the first NMOS transistor and the first PMOS transistor, the first NMOS transistor and the first PMOS transistor having respective first gates, the first gates providing respective first input nodes of the first inverter;

a second inverter having a second output node, a second NMOS transistor and a second PMOS transistor, the second output node located between the second NMOS transistor and the second PMOS transistor, the second NMOS transistor and the second PMOS transistor having respective second gates, the second gates providing respective second input nodes of the second inverter;

a third NMOS transistor and a third PMOS transistor;

a fourth NMOS transistor and a fourth PMOS transistor;

the third NMOS transistor and the fourth NMOS transistor commonly coupled to receive a first gate bias voltage;

the third PMOS transistor and the fourth PMOS transistor commonly coupled to receive a second gate bias voltage;

the third NMOS transistor having source and drain coupled between a gate of the first NMOS transistor and the second output node;

the fourth NMOS transistor having source and drain coupled between a gate of the second NMOS transistor and the first output node;

the third PMOS transistor having source and drain coupled between a gate of the first PMOS transistor and the second output node; and

the fourth PMOS transistor having source and drain coupled between a gate of the second PMOS transistor and the first output node.

2. (Original) The memory cell of Claim 1, wherein the first gate bias voltage and the second gate bias voltage are complements of one another.

3. (Original) The memory cell of Claim 1, wherein the memory cell comprises a configuration memory cell of a programmable logic device.

4. (Original) The memory cell of Claim 1, wherein the first gate bias voltage comprises a sub-threshold voltage for the third and fourth NMOS transistors, and the second gate bias voltage comprises a sub-threshold voltage for the third and fourth PMOS transistors.